

## ABSTRACT OF THE DISCLOSURE

A thin film transistor array substrate for a liquid crystal display includes an insulating substrate with a display area and a peripheral area surrounding the display area. The peripheral area has an upper region above the display area and a lower region below the display area. Signal lines are formed on the substrate such that the signal lines are bundled into a plurality of blocks. Each block has a predetermined number of signal lines. A plurality of first upper repair lines is formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines. A plurality of second upper repair lines is formed at the upper peripheral region of the substrate, crossing all of the signal lines. A plurality of first lower repair lines are formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines. The first lower repair lines cross the signal lines crossed by the first upper repair lines. A plurality of second lower repair lines is formed at the lower peripheral region of the substrate, crossing all of the signal lines. A plurality of upper connection members crosses the first upper repair lines and the second upper repair lines. A plurality of lower connection members crosses the first lower repair lines and the second lower repair lines. In this structure, even though line breakage is concentrated at a particular area, such line breakage can be collectively repaired using the spare neighboring repair lines and interconnection lines interconnecting the repair lines efficiently.

PCT/US2012/044762